ABSTRACT

A supporting structure is wafer-bonded to the upper face side of a partially or fully processed device wafer. The device wafer includes a transistor having a well region that extends into the substrate material of the device wafer. The source and drain regions of the transistor extend into the well region. After attachment of the supporting structure, the device wafer is thinned from the back side until the bottom of the well region is reached. To reduce source and drain junction capacitances, etching can continue until the source and drain regions are reached. In one embodiment, all of the well-to-substrate junction is removed in a subsequent etching step, thereby reducing or eliminating the well-to-substrate junction capacitance of the resulting transistor. Resistance between the well electrode and the transistor channel is reduced because the well contact is disposed on the back side of the device wafer directly under the transistor gate.